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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,583	07/24/2003	Kenichi Hayashi	240708US2	7738

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,583	HAYASHI ET AL	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20* is/are pending in the application.

4a) Of the above claim(s) *9-14,16,17 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,15 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/28/05 & 2/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/625583 Attorney's Docket #: 240708US2
Filing Date: 7/24/2003; claimed foreign priority to 7/26/02

Applicant: Hayashi et al.

Examiner: Alexander Williams

Applicant's RCE/Amendment filed 12/28/05 to the allowance filed 10/3/05 to the election with traverse of species of figure 1A (claims 1-8, 15, 18 and 19) filed 10/18/04 is acknowledged. This species elected read on figures 1A to 7.

This application contains claims 9-14, 16, 17 and 20 drawn to an invention non-elected with traverse.

Claim 19 has been cancelled.

Prosecution on the merits of this application is reopened on claims 1-18 and 20 considered unpatentable for the reasons indicated below:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, and with respect to claims 8, 15 and 18, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 1 to 8, 15, 18 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Saito Takehiro (Japan Patent # 63-166254) in view of Honda et al. (U.S. Patent # 6,849,805 B2).

1. Saito Takehiro (figures 1 to 6) specifically figures 3 and 4 show a semiconductor device of an insertion-mount-type comprising: a plastic package **1**; a plurality of leads **2** protruding outward from said plastic package; one or more semiconductor elements **(within the 1)** protected by said plastic package; and electric wiring **(inherent)** protected by said plastic package to connect said semiconductor elements with said leads, said semiconductor device being mounted on an external electric member **21** by inserting said leads into a lead-inserting portion **22** of said external member and joining said leads with said lead-inserting portion by solder **23**, at least one of said semiconductor elements being a power semiconductor element (inherent), wherein each of said leads includes a first lead portion **(portion of 2 closest to the package with first wide width portion)** located at a plastic package side, a second lead portion **(portion of 2 after first lead wide width portion to the beginning portion of the second wide width portion)** located at a position closer to a lead tip end than said first lead portion, and a third lead portion **(portion at the outer end of the lead 2 at the tip after the second wide width portion)** located at a position closer to the lead tip end than said second lead portion, the third lead portion being capable of being inserted into

a lead-inserting portion, the sectional area of said second lead portion is set to a value smaller than that of said first lead portion, and at least some of said leads are formed as gap controlling leads provided with gap-controlling means **(portion of 2 with the second wide portion)** to keep a gap between said semiconductor device and said external electric member constant by inserting at least some of the third lead portions being capable of being put into said external electric member up to said gap-controlling lead, said gap-controlling means being located at a position closer to the lead tip end than said second lead portion, but fail to explicitly show each of said leads being coated with solder using tin as a base material without containing lead on outside of said plastic package.

Honda et la. Is cited for showing a printed circuit board and electronic apparatus. Specifically, Honda et al. (figures 1 to 9) specifically figure 1 discloses a semiconductor device being to be mounted on an external electric member **1** by inserting said leads **2** into a lead inserting portion **5** of said external electric member and each of said leads being coated with solder **7** using tin as a base material without containing lead on outside of said plastic package for the purpose of providing exceedingly economical means for connection of integrated circuits selectively in readily removeable or permanent soldered attachment.

(2) 1. Field of the Invention

(3) This invention relates to a printed wiring board which is capable of preventing the occurrence of lift-off and land peeling at soldered portions when a component to be mounted on the printed wiring board (hereinafter referred to as the "inserted component" is soldered by using solder, in particular lead-free solder, and an electronic apparatus such as a printer in which is installed the printed wiring board.

(6) However, the high-temperature-type lead-free solders that are currently most commonly used are composed mainly of Sn and Ag, and have a melting point of about 220.degree. C. If flow soldering of an inserted component is carried out using such a high-temperature-type lead-free solder, then solidification of the solder, which is accompanied by solidification shrinkage, proceeds from the vicinity of the inserted component, which has

good thermal conductivity, towards the vicinity of the printed wiring board, and hence the solder joint interface at the part of the surface of the substrate on which the inserted component is mounted in particular becomes the final solidified part, resulting in lift-off and land peeling.

(7) Moreover, when flow soldering is carried out using lead-free solder as described above, segregation of Pb contained in the surface-treated leads of the inserted component and segregation of elements (Bismuth, etc.) contained in the lead-free solder used in the flow soldering occur during the cooling process, and the physical properties of the solder changes during the cooling process. As a result, there is a problem that the occurrence of lift-off and land peeling is increased, and in the worst cases the land peeling is accompanied by breakage (i.e., electrical disconnection) of the pattern connected to the lands.

(4) FIG. 1 is a sectional view showing a printed wiring board according to a first embodiment of the present invention in a state in which inserted component leads 2 have been flow-soldered to the printed wiring board with lead-free solder. In the present embodiment and the other embodiments described below, elements and parts corresponding to elements and parts in FIGS. 5 and 6, which show the conventional art described above, are designated by the same reference numerals as in FIGS. 5 and 6.

(7) In FIG. 1, a plurality of through holes 5 are formed in a substrate 1 of the printed wiring board, and a land 6 is formed over an inner peripheral surface of each through hole 5 and opposite end surface parts of the substrate 1 formed with each through hole 5. Inserted component leads 2 of an inserted component 3 such as an electronic component are inserted into the through holes 5 and flow-soldered to the substrate 1 with lead-free solder.

2. The semiconductor device according to claim 1, the combination with Saito Takehiro showing wherein said gap-controlling means is formed by making the lead width thereof locally larger than the width of said second lead portion.

3. The semiconductor device according to claim 2, the combination with Saito Takehiro showing wherein said leads are arranged in a line at a side portion of said plastic

package, only said leads at both ends of said line being formed as said gap-controlling leads.

4. The semiconductor device according to claim 2, the combination with Saito Takehiro showing wherein the thickness of said first lead portion is equal to that of said second lead portion, the width of said second lead portion being smaller than that of said first lead portion.

5. The semiconductor device according to claim 2, the combination with Saito Takehiro showing wherein the sectional area of said second lead portion is equal to that of said third lead portion.

6. The semiconductor device according to claim 2, the combination with Saito Takehiro showing wherein said gap-controlling means is formed in a shape protruding to both directions along a lead width direction.

7. The semiconductor device according to claim 6, the combination with Saito Takehiro showing wherein the lead width of said gap-controlling means is equal to that of said first lead portion.

8. The semiconductor device according to claim 7, the combination with Saito Takehiro showing wherein each of said gap-controlling leads is formed by linearly cutting said lead frame having a wide portion corresponding to said first lead portion, a narrow portion corresponding to said third lead portion, and a tie bar portion which connects said wide portion with said narrow portion and in which two holes are formed, and both of said holes are located at both sides of a range of said narrow portion along the lead width direction so that said holes are not present in said range, said holes being located on extension lines of both sides of said wide portion.

15. The semiconductor device according to claim 8, the combination with Saito Takehiro showing wherein each of said holes is a rectangular hole in which two opposite sides are parallel with the lead width direction or lead extending direction.

18. The semiconductor device according to claim 2, the combination with Saito Takehiro showing wherein each of said gap-controlling leads is formed by linearly cutting said lead frame having a wide portion corresponding to said first lead portion, a narrow portion corresponding to said third lead portion, and a tie bar portion which connects said wide portion with said narrow portion and in which two cutoff are formed at a position closer to said narrow portion, and said cutoffs are located at both sides of a range of said narrow portion in a lead width direction, said cutoffs being located on

extension lines of both sides of said wide portion so as to be previously provided with said gap controlling means.

19. The semiconductor device according to claim 1, the combination with Saito Takehiro showing wherein each of said leads is coated with solder using tin as a base material without containing lead.

Therefore, it would have been obvious to one of ordinary skill in the art to use Honda et al.'s leads attachment to modify Saito Takehiro's leads for the purpose of providing exceedingly economical means for connection of integrated circuits selectively in readily removeable or permanent soldered attachment.

As to the grounds of rejection under section 103, see MPEP § 2113.

Response

Applicant's arguments filed 12/28/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

Field of Search	Date
U.S. Class and subclass: 257/666,696,698,691,690,693,692,776,775,787,673,672,671,670,e23.043 361/774,748,761,776,405 439/75 228/180 174/52.4	12/24/04 6/14/05 5/15/06
Other Documentation: foreign patents and literature in 257/666,696,698,691,690,693,692,776,775,787,673,672,671,670,e23.043 361/774,748,761,776,405 439/75 228/180 174/52.4	12/24/04 6/14/05 5/15/06
Electronic data base(s): U.S. Patents	12/24/04 6/14/05 5/15/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/15/06